

VERSION SHOWING AMENDMENTS TO THE CLAIMS

(AS PER AMENDED SHEET)

This listing replaces all prior listings of the claims.

IN THE CLAIMS

Amend the claims as follows:

1 (Currently amended). An organic field effect transistor (OFET) including a gate, comprising:

~~which comprises at least a first electrode layer having~~ forming a source or and drain electrode[[s]] and having multiple sides (1, 2 and 5, 7);

a semiconducting layer[[,]]

an insulator layer; and

a second electrode layer forming the other of said source and drain electrodes (8 and 13), and in which one of and having multiple sides wherein the source or drain electrode[[s]] (source or drain) in the first electrode layer surrounds the respective other electrode of the second electrode layer in a two-dimensional manner with the exception of one of said sides or location of the other electrode (the connection side or location) of this electrode;

~~characterized in that~~

whereby a u-shaped and/or meandering current channel (3, 6), which begins and ends on one of said sides of the an electrode of the first electrode layer, can be is formed in the semiconducting layer.

2 (Currently amended). The OFET as claimed in claim 1 wherein, in which

2 (Currently amended). The OFET as claimed in claim 1 wherein, ~~in which~~
~~one of~~ the first electrodes layer respectively bounds the other electrode
layer on three of four sides.

3 (Currently amended). The OFET as claimed in ~~either of the preceding~~
claim 1 ~~claims 1 and 2, in which~~ wherein the second electrode layer
completely covers the current channel of the first electrode layer and, in
addition, at least one other part of ~~one of~~ the first electrode layer s, this
other additionally covered part having a width in the range from 0 to 20 μm
and having a length in the range of the length of the current channel.

4 (Currently amended). The OFET as claimed in claim 1 wherein ~~one of~~
~~the preceding claims~~, holes and/or interruptions are being present in the
semiconductor layer ~~in order~~ to reduce leakage currents.

5 (Currently amended). An integrated circuit having at least two OFETs as
claimed in claim 1 ~~in one of the preceding claims, wherein~~ the at least two
OFETs are being arranged into a the NAND or NOR gate in such a manner
that the one sides of the two OFETs ~~connection sides or locations~~ are
respectively opposite one another.

6 (Currently amended). The integrated circuit as claimed in claim 5,
including the connecting lines and/or the inputs and outputs respectively
being situated in a the region between the one sides ~~connection sides or~~

7 (Currently amended). The integrated circuit as claimed in ~~either of claims 5 and 6, claim 5 wherein~~ holes and/or interruptions are ~~being provided~~ in the semiconductor layer.

8 (Currently amended). The integrated circuit as claimed in claim 7 ~~wherein,~~ the holes and/or interruptions are ~~being situated~~ between the one sides ~~connection sides or locations~~.

9 (Currently amended). The integrated circuit as claimed in claim 5 ~~one of claims 5 to 8, use being made of~~ including a through-contact in said first electrode layer ~~instead of at least one electrical connection~~.

10 (Currently amended). The integrated circuit as claimed in claim 9 ~~[[,]]~~ wherein the through-contact extends ing at least to ~~as far as~~ one further side of the OFET other than said one side ~~(10b)~~.

Add the following claims:

11 (New). The OFET as claimed in claim 2 wherein the second electrode layer completely covers the current channel of the first electrode layer and, in addition, at least one other part of the first electrode layer, this other additionally covered part having a width in the range from 0 to 20 μm and having a length in the range of the length of the current channel.

12 (New). The OFET as claimed in claim 2 wherein holes and/or interruptions are in the semiconductor layer to reduce leakage currents.

13 (New). The OFET as claimed in claim 3 wherein holes and/or interruptions are in the semiconductor layer to reduce leakage currents.

14 (New). An integrated circuit having at least two OFETs as claimed in claim 2 wherein the at least two OFETs are arranged into a NAND or NOR gate such that the one sides of the two OFETs are respectively opposite one another.

15 (New). An integrated circuit having at least two OFETs as claimed in claim 3 wherein the at least two OFETs are arranged into a NAND or NOR gate such that the one sides of the two OFETs are respectively opposite one another.

16 (New). An integrated circuit having at least two OFETs as claimed in claim 4 wherein the at least two OFETs are arranged into a NAND or NOR gate such that the one sides of the two OFETs are respectively opposite one another.

17 (New). The integrated circuit as claimed in claim 14 including connecting lines and/or inputs and outputs respectively situated in a region between the one sides.

18 (New). The integrated circuit as claimed in claim 15 including connecting lines and/or inputs and outputs respectively situated in a

region between the one sides.

19 (New). The integrated circuit as claimed in claim 16 including connecting lines and/or inputs and outputs respectively situated in a region between the one sides.

20 (New). The integrated circuit as claimed in claim 17 including connecting lines and/or inputs and outputs respectively situated in a region between the one sides.